ABSTRACT

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) is highly energy efficient because of its simple architecture.SAR ADC is most popular its for low to moderate resolution.In SAR, the main key linearity limiting factor is capacitor mismatch and comparator offset. In this thesis, redundant SAR ADC is implemented with several new contributions in offset cancellation technique. The main contribution in this thesis includes analysis of error correction techniques (redundancy) for correcting errors due to manufacturing mismatches (capacitor mismatch), design of new architecture to have redundancy within architecture also achieving 94% energy efficiency compared to conventional switching techniques, developing a single stage dynamic latch comparator to achieve offset well below tolerable limit by introducing new calibration logic for offset nullification.

This work tries to fulfill the specification by implementing SAR ADC in SCL 180nm technology(Semi-conductor Laboratory). The converter has been implemented by using redundancy scaled capacitive digital to analog converter architecture showing $\sigma(DNL) \approx 0.1LSB$ at sampling rate of 10kS/s in MATLAB model with non ideal capacitor.