ABSTRACT

The economic benefits of device scaling drive the semiconductor industry to push the limits of innovation. In the era of smart gadgets, the demands are application-specific like radiation hardened design, Internet of Things (IoT) devices, low power devices and accelerator circuits. These needs lead to innovative device design with high performance CMOS technologies. The UTBB FDSOI is such a promising technology for sub-10nm CMOS nodes. However, the variability is one of the major issues, the industry faces today. In this thesis, we have studied the impact of variability sources like line edge roughness, metal-gate granularity, floating body thickness and buried oxide (BOX) layer thickness on the threshold voltage of the UTBB FDSOI transistors. Our work demonstrates that the ground plane doping is beneficial to compensate for the effect of line edge roughness.