ABSTRACT

Charge Coupled Devices (CCDs) are the most common image sensors used in space applications due to their higher dynamic range, better quantum efficiency and uniformity. The CCDs generate measurable charge using incident photons. The charges are read by moving the charge collected on each exposed pixel to the output amplifier. This charge transfer process is accomplished by applying a High Voltage (HV) clock at each pixel electrode of CCD. The charge transfer process performance depends on the rise/fall time and frequency of the HV clock. However, the CCDs offer a significant amount of capacitance (in the range of nF) to the driver circuit, making it difficult to meet rise/fall time constraint due to demand of a huge drive current. The conventional low voltage devices are not preferred for high voltage and high current operation as it may lead to hot switching, breakdown and reliability issues. The Laterally Diffused Metal Oxide Semiconductor (LDMOS) devices are typically used to serve this application.

In this work, we have designed a clock driver circuit using indigenous LDMOS transistors. The clock driver circuit design consists of a driver and a pre-driver stage. The HiSIM-HV2 model is used to implement driver stage using 20 V NLDMOS and PLDMOS transistors. However, pre-driver stage consisting of a floating High Voltage Level Shifter (HVLS) stage and a buffer stage is implemented using conventional 3.3 V devices of SCL's 180 nm PDK. The designed 20 V clock driver has a rise and fall time of around 6 to 7 ns for the given load of 850 pF and can operate at a frequency of 10 MHz. The designed circuit is verified at various process corners and found to be working without any issue.