ABSTRACT

Circuits operate in radiation active environments such as space, nuclear power plant, etc. are to be designed with high precision and extra care as they may be irradiated. These radiations can temporary or permanent damage the design. Hard-errors cause physical damage to ICs which are irreversible and hard to deal with, however plenty of approaches have been proposed to deal with soft-errors.

In this work, a novel soft error tolerant design has been presented which is compared with state of the art cells on basis of various energy efficient metrics. The design outperforms the existing designs in terms of Read Energy and Delay requirement. It also outperforms other designs on basis of low voltage operation. We have implemented all the designs in UMC 28nm CMOS technology. We report that The proposed design has 65.5%(72%),-33%(-88%),75.2%(93.03%), and 72.5%(61.8%) lesser read-energy$\times$delay-product and write-energy$\times$delay-product when compared with DICE , NS10T, RSP14T, and RHPD12T SRAM respectively in a 16$\times$4 array. Post layout Simulations were also done to discuss the energy efficiency of the design. Next based on the proposed ERDP-DICE cell, a new design DNUDPSRAM(Double Node Upset Hardened Dual port SRAM cell) is proposed which essentially has the main aim to make the cell robust and tolerant to DNU. Extensive Simulations using double exponential current source models have been done to verify the Hardening of the proposed cell.

Every phase in the chip-design process has multiple stages, carried

out by different designers and hence, the opportunities for ambiguity and error in the hardware design are rife. Verification is the process of guaranteeing that each level of implementation adheres to the intended functionality of the module. Therefore we also propose a novel Industry standard methodology to verify the functionality of the design at RTL level using Formal Verification. Here, a data memory is coded in System Verilog and Formal Property Verification(FPV) is done to verify the functionality of the design. The formal coverage achieved was 100% here.