ABSTRACT

The analog circuits are an inherent part of any modern integrated circuit. However due to scaling limitations, there are many challenges to integrate these circuits into the modern system-on-chip (SoC) designs. In the last decade, there are several studies on the analog performance of modern semiconductor devices like FinFETs. The drain saturation voltage ($V_{DS,SAT}$) is an essential FoM for analog circuit performance as it provides the information about biasing and swing. In this thesis, We used G-function technique to extract the $V_{DS,SAT}$ as it is independent of the geometry of device and versatile in nature. The analysis is primarily focused on the variation of $V_{DS,SAT}$ with different gate lengths (L_G), fin widths (W_{Fin}) and spacer materials of different dielectric constants (K). The key points of this work are: $V_{DS,SAT}$ is grater than overdrive voltage (V_{OV}) in sub-10nm W_{Fin} due to resistive drop and mobility degradation. The $V_{DS,SAT}$ is more for FinFETs with high dielectric constants (K) spacer material.