ABSTRACT

Circuits that need to operate in harsh environments such as in space, military, nuclear reactors, etc. need to be designed carefully as they are subjected to external irradiations. In this context, Radiation Hardening By Design(RHBD) has gained much importance in the last couple of decades. Radiations can lead to temporary or permanent failures in the designs. While hard-errors such as Total Ionization Dose (TID), which cause physical damage to ICs are hard to deal with, plenty of approaches have been proposed to deal with soft-errors.

DICE and Quatro are prominently used SRAM cells for space application. In a given power budget provided for a space-craft/satellite, Qutaro/DICE SRAM memory consumes significant amount of power. In this thesis, Read-decoupled DICE and Read-Decoupled Quatro cells have been purposed that consumes maximum 0.2 $\times$ Read energy compared to conventional DICE and Quatro SRAM cells and a comparative study has also been presented between the purposed cells and conventional DICE and Quatro which shows that the proposed designs have high read and write stability under severe process variation. The simulation results are realized in UMC-65 nm Technology via Cadence Virtuoso tool. Layout is drawn in Mentor Graphics integrated with cadence. To make simulation time-efficient, whole process of analysis and extraction of results of the designs has been completed automated through OCEAN script.

SRAM cell layout is drawn in UMC 65-nm and SCL 180-nm technology. To design a memory of various size, an in-house Memory compiler is designed. We used SKILL-script to design memory compiler which takes a cell layout as a input and provides the required memory array. The purpose of compilers is to auto-

matically generate various kinds of memories depending on the customer order. The compiler design flow for schematic and layout generation has been design and presented in this thesis.

Guard band helps in reducing radiation effects (Single event transient (SET), Single event upset(SEU), Total Ionization dose (TID) and Single event latch-up). To reduce the radiation effects in conventional SRAM cell like 6-T, 8-T, DICE and Quatro, guard band is added and laid out in SCL-180 nm Technology. The memory array of each of the above cell is built using in-house designed memory complier. The design memory will be fabricated by SCL-180 nm Foundry Chandigarh.