ABSTRACT

Radiation robust circuit design for harsh environments like space is a big challenge for today researchers. As circuits become more and more complex and CMOS processes get denser, it is observed that their immunity towards particle strike decreases drastically. The existing work on radiation hardened techniques has mostly focused on masking the radiation strikes using redundancy either spatial or temporal which consume more power, area and give the lesser performance as compared to unhardened design. Also, the existing radiation hardened techniques such as Triple Modular Redundancy (TMR), Guarded Dual Modular Redundancy (GDMR), Glitch filtering (GF) is not compared at the processor level. In this work, we have implemented these techniques on a 3-stage MIPS based Plasma processor and an automated flow is designed which converts each of the above mentioned techniques from a unhardened design to a radiation immune processor. A comparison is done in terms of area, power, and performance and it is shown that GDMR technique is an optimized solution as it consumes less area and power compared to TMR and has less performance penalty compared to GF.

In this work, we have also proposed two novel radiation-hardened design techniques, Timing-aware Radiation Hardened Design (TRHD) and Soft Error Resilient Asynchronous Design (SERAD) which use error detection and correction methods to correct the radiation strike. As error detection & correction techniques pay the penalty only when SET occurs, the proposed techniques have similar performance compared to unhardened design. The former design is based on a synchronous technique which borrows time from the next stage to correct the SET occurring in a processor whereas the latter is based on asynchronous bundled

data. It detects the SET and re-samples the data on the occurrence of SET. Both of these designs are inspired from the timing resilient designs. SERAD technique has lesser area and delay penalty than TMR, GDMR and GF. All the designs have been implemented in open source NCSU 45nm technology. The area of SERAD Plasma design is 71% more than the synchronous Plasma which is lesser than TMR, GDMR and glitch filtering. The delay overhead in SERAD plasma only incurs in the presence of a SET (whose probability of occurrence is very less) and frequency of operation is comparable to the synchronous Plasma (only 2 % lesser).