ABSTRACT

The image sensor is one of the important circuit in the microelectronics industry. Most of the scientific instruments used in space missions employ cameras. In space applications, the scientific cameras generally demand exceptional performance and operate under very harsh conditions. Hence, the sensor unit requires a very special design to provide high-quality images that are free from noise. Most of the space applications use charge-coupled devices (CCDs) as the sensor element. The qualities of CCD degrade when exposed to radiation but they can still be used with high performance. However, the problem with CCD imager is the readout noise. To eliminate the noise coming from the channel, dedicated hardware called signal processing circuits are needed. The signal processing circuit consists of correlated double sampling (CDS) to remove the reset noise (KTC noise) and offset error from the output of CCD signal. This technique moreover enhances the image quality by improving the noise floor of the collected light from the sensors.

In this work, a 16-bit, 1 MSPS CDS circuit with the programmable gain feature is designed using 180nm CMOS technology. The Analog Front End (AFE) is implemented by using a single amplifier. Since designing with sub-micron CMOS technology is very challenging, every block of the circuit has been presented as a design procedure adhering to the design constraints. A state of art amplifier with a gain of 130 dB and UGB of 15MHz is also presented. The switched capacitor network and its high-speed integration with the operational transconductance amplifier (OTA) is also discussed in detail. The designed circuit is tested under normal/worst case working conditions and shown to be working within the specification.