ABSTRACT

Content Addressable Memories (CAMs) are high-speed hardware search engines that simultaneously perform a parallel search across the rows. This high speed, however, comes at the cost of increased power. In this thesis we present two different CAM designs, one for low EDP suitable for low energy applications, and radiation hardened CAM suitable for space applications.

In CAMs, most of the power is consumed in the charging and discharging of the long matchlines. Although precharge-free CAMs eliminate the excessive power consumption due to the matchlines, they are comparatively slower than conventional CAMs. In this thesis we have studied the existing precharge-free CAMs (PFCAMs) and implemented a novel PFCAM in UMC 28nm technology. Extensive Monte-Carlo simulations carried out to study the correctness of the PFCAMs show that existing precharge-free CAMs give false search results under process variations. In this thesis, we implement a robust and energy-efficient pseudo-precharge-free CAM. We have carried out detailed schematic and layout simulations for the proposed PFCAM along with all the peripheral circuits. For an array size of 32×32, the proposed design shows $\sim285\times$ energy-delay-product reduction compared to the existing precharge-free CAMs. In comparison with NOR-type CAM, the proposed design has $\sim2.7\times$ of energy-delay-product reduction for the array size of 32×32. For the same array size, the proposed design has $\sim1.85\times$ delay reduction and $\sim1.5\times$ energy reduction as compare to NOR CAM respectively. For the 32×32 array, post layout simulation of proposed design shows us $\sim1.74\times$ energy delay product, $\sim1.7\times$ energy efficient and $\sim1.5\times$ search delay reduction as compare to NOR-CAM. .

CAMs used in space applications have to be free from errors occurring due to radi-